Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OUTPUT**
2. **V-**
3. **V+**
4. **INPUT –**
5. **INPUT +**

**.035”**

**3**

**2**

**1**

**4**

**5**

**MASK**

**REF**

**LMH6624**

**A**

**.032”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0035” X .0035”**

**Backside Potential: V-**

**Mask Ref: LMH6624 A**

**APPROVED BY: DK DIE SIZE .032” X .035” DATE: 9/7/23**

**MFG: NATIONAL THICKNESS .010” P/N: LMH6624**

**DG 10.1.2**

#### Rev B, 7/1